REMARKS

Claims 1-29 are pending in this application.

Claims 1-29 have been rejected.

Reconsideration and full allowance of Claims 1-29 are respectfully requested.

I. AMENDMENTS TO THE SPECIFICATION

The Applicant has amended two paragraphs in the specification to correct typographical errors. No new matter has been added to the specification as a result of these amendments.

II. OBJECTION TO THE DRAWINGS

On Page 3 of the May 20, 2004 Office Action the Examiner objected to FIGURE 1 of the drawings stating that FIGURE 1 should be designated by a "Prior Art" legend because "only that which is old is illustrated." The Applicant respectfully traverses this objection of the Examiner for the following reasons.

FIGURE 1 has not been labeled "Prior Art" because FIGURE 1 depicts an embodiment of the present invention. The specification states that "FIGURE 1 illustrates an exemplary processing system capable of determining the memory requirements of an embedded system under design according to one embodiment of the present invention." (Specification, Page 8, Lines 6-8). In addition, the specification states that "FIGURE 1 illustrates exemplary processing system 100, which is capable of designing and optimizing the memory of an embedded system, such as an application specific integrated circuit (ASIC), according to one embodiment of the present

invention." (Specification, Page 9, Lines 9-12). The specification goes on to describe the memory design and optimization application programs and data files that reside in memory 120. The specification clearly describes the system 100 shown in FIGURE 1 as a system that embodies the present invention. For this reason the system 100 shown in FIGURE 1 is not a prior art system.

Therefore, the Applicant respectfully submits that no amendment of FIGURE 1 is required. The Applicant respectfully requests the Examiner to withdraw the objection to FIGURE 1 in view of the Applicant's comments set forth above.

III. REJECTIONS UNDER 35 U.S.C. § 112

On Pages 3-4 of the May 20, 2004 Office Action the Examiner rejected Claims 1-29 under 35 U.S.C. § 112, first paragraph, for allegedly failing to comply with the written description requirement. In particular, the Examiner asserted that "The claims(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." (May 20, 2004 Office Action, Page 4, Lines 6-9). The Applicant respectfully traverses this assertion of the Examiner. The Applicant respectfully submits that the subject matter of the claims is properly described for the reasons set forth below.

The Examiner stated that there is "not enough information" in the specification and drawings of the patent application regarding "a simulation controller," a "memory access monitor," and a "memory optimization controller" as claimed in Claim 1. (May 20, 2004 Office Action, Page 4, Lines 12-22). The Applicant also respectfully traverses this assertion.

To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor has possession of the claimed invention. (MPEP § 2163).

A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. The examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description. The examiner has the initial burden of presenting by a preponderance of the evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. (MPEP § 2163).

In rejecting a claim, the examiner must set forth express findings of fact regarding the above analysis which support the lack of written description conclusions. A general allegation of "unpredictability in the art" is not a sufficient reason to support a rejection for lack of adequate written description. (MPEP § 2163).

In the present case a general allegation of "not enough information" is also an insufficient reason to support a rejection for lack of adequate written description. The Applicant respectfully submits that the specification does contain "enough information" for an adequate written description of the claimed subject matter.

The MPEP states that the subject matter of a claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement. (MPEP § 2163.02). Therefore, in the present case, it is not necessary that the specific words "a simulation controller," a "memory access monitor," and a "memory optimization

controller" appear in that form in the specification. The question is whether the concepts and structures expressed by these words appear in the specification. The Applicant respectfully submits that they do.

The Applicant respectfully directs the Examiner's attention to the following portion of the specification: "[T]he term 'controller' means any device, system or part thereof that controls at least one operation, such a device may be implemented in hardware, firmware or software, or some combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether locally or remotely." (Specification, Page 7, Lines 10-16).

The word "simulation" has been added to the word "controller" to describe the portions of software that are executed in the hardware that perform the simulation operations. The specification identifies software modules that simulate a program (e.g., instruction set simulator (ISS) program, simulated ASIC memory space 230). "ISS program 220 simulates the execution of the compiled object code by the target device in simulated ASIC memory space 230." (Specification, Page 13, Lines 18-20). The other software modules identified in the specification (e.g., debugger program 235) may also be used in the simulation operation. "As the execution of the object code is simulated, debugger 235 is capable of working with ISS program 220 to permit the designer to track the simulated execution of the object code." (Specification, Page 14, Lines 1-4).

Further, it is clear that the various software modules can be combined in any order. "It should be noted that the exemplary programs depicted in memory 120 reflect only one possible logical division of the functions of a memory design tool according to the principles of the present

invention." (Specification, Page 12, Line 21 to Page 13, Line 3). Therefore, in view of the definition of the term "controller" and the simulation operations described in the specification, the specification reasonably conveys to a person skilled in the art the concept and structure and operation of a "simulation controller." The specific words "simulation controller" that appear in the claims are fully explained and supported in the specification in a manner that reasonably conveys to a person skilled in the art that the Applicant has possession of the claimed invention at the time the patent application was filed.

Similarly, the terms "memory access monitor" and "memory optimization controller" are also explained in the specification. "As the execution of the object code is repeatedly simulated, ISS program 220 monitors all memory access operations and creates in the histogram file 250 a plurality of histograms of all memory access operations." (Specification, Page 14, Lines 5-8). Therefore, the specification clearly supports the concept sand structure and operation of a "memory access monitor." "Memory design and optimization program 280 uses the data in histogram 250, the data in memory models file 260, and the data in user design criteria file 270 to determine the types and amounts of memory that should be used in the target device to best meet the operating parameters specified by the user in user design criteria file 270." (Specification, Page 14, Lines 17-22). Therefore, the specification clearly supports the concept sand structure and operation of a "memory optimization controller."

In view of the foregoing remarks, the Applicant respectfully submits that the burden of the Patent and Trademark Office has not been met to establish (by a preponderance of the evidence) a valid reason for supporting a rejection for lack of adequate written description. Therefore, the

Applicant respectfully requests the Examiner to withdraw the rejections that are based on a supposed lack of adequate written description.

On Pages 4-5 of the May 20, 2004 Office Action the Examiner rejected Claims 1-7 under 35 U.S.C. § 112, second paragraph, for allegedly being "indefinite" due to the use of the term "capable." The Applicant respectfully traverses these rejections. The Applicant respectfully submits that the term "capable" is not a relative term and that the meaning of the term "capable" is well known and that the phrase "capable of" is extensively used in patent documents. The Examiner has cited no authority for the assertion that the term "capable" is indefinite.

The Applicant has searched the United States Patent and Trademark Office database for uses of the phrase "capable of" in at least one claim of an issued United States patent during the issuing period from January 1, 2000 through July 31, 2004, and identified 56,832 patents. The phrase "capable of" is commonly used in claim limitations and is commonly accepted by the United States Patent and Trademark Office. The Applicant respectfully submits that the phrase "capable of" in a claim limitation is, in point of fact, definite and that the use of the phrase "capable of" in a claim limitation does not render the claim limitation indefinite.

In view of the foregoing remarks, the Applicant respectfully submits that the burden of the Patent and Trademark Office has not been met to establish that the phrase "capable of" in a claim limitation is indefinite. Therefore, the Applicant respectfully requests the Examiner to withdraw the rejections that are based on a supposed indefiniteness with respect to the use of the term "capable" in a claim limitation.

IV. REJECTIONS UNDER 35 U.S.C. § 103

In Paragraph 6.1 of the May 20, 2004 Office Action the Examiner rejected Claims 1, 5, 6, 8, 12, 13, 15, 19, 20, 22, 26, 28 and 29 under 35 U.S.C. § 103(a) as being unpatentable over Gupta et al., "Processor Evaluation in an Embedded Systems Design Environment" ("*Gupta*") in view of a printed publication by Prete et al. entitled "The ChARM Tool For Tuning Embedded Systems ("*Prete*").

The Applicant respectfully points out that the Examiner incorrectly stated that Gupta et al. was "(Inventor of instant application)." (May 20, 2004 Office Action, Page 5, Paragraph 6.1, Line 3). The person named Gupta in the prior art reference is T. Vinod Kumar Gupta. The inventor of the present invention is Vidyabhusan Gupta.

In Paragraph 6.2 of the May 20, 2004 Office Action the Examiner also rejected Claims 2-4, 7, 9-11, 14, 16-18, 21, 23-25 and 28 under 35 U.S.C. § 103(a) as being unpatentable over *Gupta* and *Prete* in view a printed publication by Dutt et al. entitled "Hot topic session: How to solve the current memory access and data transfer bottlenecks: at the processor architecture or at the compiler level?" ("*Dutt*"). The Applicant respectfully traverses these rejections.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed.Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed.Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed.Cir. 1984). Only when a *prima facie* case of obviousness is

established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed.Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed.Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed.Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed.Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed.Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on the applicant's disclosure. MPEP § 2142.

Gupta describes a methodology for embedded systems design for vision/image processing applications. (*Gupta*, Page 3, Second paragraph, Lines 1-2). The objective of *Gupta* is to evaluate a range of target processors using an "application behavior specification" to determine the processors' suitability for use. (*Gupta*, Page 3, Third paragraph, Lines 1-2). *Gupta* characterizes and evaluates "processor architectures." (Gupta, Page 3, Third paragraph, Lines 4-5).

Claim 1 of the patent application presently reads as follows:

> 1. (Previously Presented) An apparatus for designing a memory for use in an embedded processing system comprising:
>
> a simulation controller capable of simulating execution of a program to be executed by said embedded processing system;
>
> a memory access monitor capable of monitoring memory accesses to a simulated memory space during said simulated execution of said program, wherein said memory access monitor is capable of generating memory usage statistical data associated with said monitored memory accesses, and wherein said memory accesses comprise read operations and write operations; and
>
> a memory optimization controller capable of comparing said memory usage statistical data and one or more design criteria associated with said embedded processing system and, in response to said comparison, determining at least one memory configuration capable of satisfying said one or more design criteria.

Claim 1 recites a simulation controller that is capable of simulating execution of a program to be executed by an embedded processing system. The *Gupta* reference does not disclose a simulation controller of the type described and claimed by the Applicant. As the Examiner has previously stated, "*Gupta* fails to explicitly disclose a simulation controller that is capable of simulating execution of a user program." (December 7, 2003 Office Action, Page 4, Lines 9-10).

Claim 1 also recites a memory access monitor that is capable of "monitoring memory accesses to a simulated memory space" during "simulated execution" of a program, where the memory accesses include "read operations and write operations."

Section 5.4 of *Gupta* recites a "memory bandwidth requirement" module that "computes the ratio of the number of input-output instructions to the total number of instructions." (*Gupta*, Page 25, Last paragraph, Lines 1-2). This portion of *Gupta* simply recites that the number of input-outputs are counted and the total number of instructions are counted. This portion of *Gupta* lacks any mention of monitoring "memory accesses" to a "simulated memory space" during "simulated

execution" of a program, where the memory accesses include "read operations and write operations" as recited in Claim 1.

Claim 1 also recites a memory optimization controller capable of comparing "memory usage statistical data" produced by the memory access monitor to one or more "design criteria" to determine at least one "memory configuration" capable of satisfying the design criteria.

Figure 2.1 of *Gupta* simply illustrates the overall methodology of *Gupta*. This portion of *Gupta* lacks any mention of comparing "memory usage statistical data" to one or more "design criteria" as recited in Claim 1. Moreover, this portion of *Gupta* lacks any mention of determining at least one "memory configuration" capable of satisfying design criteria as recited in Claim 1. In particular, the objective of *Gupta* is to evaluate target processors. *Gupta* contains no mention of determining any type of "memory configuration" as recited in Claim 1.

The Examiner has stated that "The *Gupta* reference does not expressly teach comparing memory usage statistical data and one or more design criteria associated with the embedded processing system to determine at least one memory configuration capable of satisfying one or more design criteria." (May 20, Office Action, Page 7, Lines 1-4).

The Examiner has stated that Claims 1, 5, 6, 8, 12, 13, 15, 19, 20, 22, 26, 28 and 29 are obvious over the *Gupta* reference in view of the *Prete* reference. (May 20, 2004 Office Action, Page 8, Lines 1-8). The Applicant respectfully traverses the Examiner's assertion that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system as taught by *Gupta* include elements as taught by *Prete*.

First, the supposed motivation to obtain "in order to balance conflicting requirements

(design criteria)" (May 20, 2004 Office Action, Page 8, Lines 5-6) is very general and does not specifically suggest combining the teachings of the *Prete* reference with the teachings of the *Gupta* reference. There must be some suggestion or motivation, either in the references themselves, or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. The desire to obtain "a balance of conflicting requirements of design criteria" is too general and vague to provide the requisite motivation to modify a reference or to combine reference teachings.

In order to establish obviousness by combining references there must be some teaching or suggestion in the prior art to combine the references. *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed.Cir. 1997) ("It is insufficient to establish obviousness that the separate elements of an invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the references."); *In re Rouffet*, 149 F.3d 1350, 1355-56, 47 USPQ2d 1453, 1456 (Fed.Cir. 1998) ("When a rejection depends on a combination of prior art references, there must be some teaching, or motivation to combine the references.")

Evidence of a motivation to combine prior art references must be clear and particular if the trap of "hindsight" is to be avoided. *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed.Cir. 1999) (Evidence of a suggestion, teaching or motivation to combine prior art references must be "clear and particular." "Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence.'"). *In re Roufett*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed.Cir. 1998) ("[R]ejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together

elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be 'an illogical and inappropriate process by which to determine patentability.'")

The Applicant respectfully submits that the alleged motivation to combine references presented by the Examiner does not meet the legal requirement to establish a finding of *prima facie* obviousness. The Applicant respectfully submits that the alleged motivation to combine references is not clear and particular. The fact that two references are concerned with the same general technical area does not, without more, provide a "clear and particular" motivation to combine the references. The Applicant respectfully submits that the alleged motivation to combine references has been assumed by "hindsight" in light of the existence of the Applicant's invention.

With respect to the rejection of Claims 5, 12, 19 and 26, these claims are directed to simulating the execution of a program N times. The Examiner stated that "*Gupta* does not expressly teach running the program N times." (May 20, 2004 Office Action, Page 8, Line 20). The Examiner asserted that this deficiency of *Gupta* may be remedied by combining the *Gupta* reference and the *Prete* reference "in order to reduce the variations in the parameter values." (May 20, 2004 Office Action, Page 9, Lines 1-6). The Applicant respectfully submits that the supposed motivation to combine the two references is legally insufficient for the reasons that have been previously set forth. The desire to obtain "reduce the variations in the parameter values" is too general and vague to provide the requisite motivation to modify a reference or to combine reference teachings.

With respect to the rejection of Claims 6, 13, 20 and 27, these claims are directed to determining at least one figure of merit associated with at least one memory configuration.

The Examiner stated that "*Gupta* fails to explicitly teach performance results specific to memory configuration." (May 20, 2004 Office Action, Page 9, Lines 18-19). The Examiner asserted that this deficiency of *Gupta* may be remedied by combining the *Gupta* reference and the *Prete* reference "to aid a designer in selecting/rejecting a particular processor architecture." (May 20, 2004 Office Action, Page 9, Lines 27-28). The Applicant respectfully submits that the supposed motivation to combine the two references is legally insufficient for the reasons that have been previously set forth. The desire to obtain "to aid a designer in selecting/rejecting a particular processor architecture" is too general and vague to provide the requisite motivation to modify a reference or to combine reference teachings.

With respect to the rejection of Claim 29, this claim is directed to generating memory usage statistical data comprising histograms. The Examiner stated that "*Gupta* does not expressly teach generating histograms to illustrate memory usage statistical data based on variable names contained in the program to be executed by the embedded system or memory locations accessed by said program." (May 20, 2004 Office Action, Page 10, Lines 10-12). The Examiner asserted that this deficiency of *Gupta* may be remedied by combining the *Gupta* reference and the *Prete* reference "in order to fine-tune the memory subsystem configuration." (May 20, 2004 Office Action, Page 10, Line 19 to Page 11, Line 2). The Applicant respectfully submits that the supposed motivation to combine the two references is legally insufficient for the reasons that have been previously set forth. The desire to "fine-tune the memory subsystem configuration" is too general and vague to provide the requisite motivation to modify a reference or to combine reference teachings.

For the reasons set forth above, a *prima facie* case of obviousness against Claims 1, 5, 6, 8, 12, 13, 15, 19, 20, 22, 26, 28 and 29 has not been established. Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejections and full allowance of Claims 1, 5, 6, 8, 12, 13, 15, 19, 20, 22, 26, 28 and 29.

In Paragraph 6.2 of the May 20, 2004 Office Action the Examiner also rejected Claims 2-4, 7, 9-11, 14, 16-18, 21, 23-25 and 28 under 35 U.S.C. § 103(a) as being unpatentable over *Gupta* and *Prete* in view a printed publication by Dutt et al. entitled "Hot topic session: How to solve the current memory access and data transfer bottlenecks: at the processor architecture or at the compiler level?" ("*Dutt*"). The Applicant respectfully traverses these rejections.

With respect to the rejection of Claims 2, 9, 16 and 23, these claims are directed to determining at least one memory configuration from a set of memory types. With respect to the rejection of Claims 3, 4, 10, 11, 17, 18, 24 and 25, these claims are directed to specifying at least one memory configuration comprising a first memory type and a first memory size, a second memory configuration comprising a second memory type and a second memory size.

The Examiner stated that "*Gupta* does not expressly teach the details of the identified processor architecture such as memory type and configuration." (May 20, 2004 Office Action, Page 12, Lines 8-9). The Examiner asserted that this deficiency of *Gupta* may be remedied by combining the *Prete* reference and the *Dutt* reference "in order to balance conflicting requirements (design criteria)." (May 20, 2004 Office Action, Page 13, Lines 15-16). The Applicant respectfully submits that the supposed motivation to combine the three references is legally insufficient for the reasons that have been previously set forth. The desire to obtain "to balance conflicting requirements

(design criteria)" is too general and vague to provide the requisite motivation to modify a reference or to combine reference teachings.

With respect to the rejection of Claims 7, 14, 21 and 28, these claims are directed to a code optimization controller capable of modifying a program in response to a comparison of memory usage statistical data and one or more design criteria to thereby enable an embedded processing system to execute the program according to one or more design criteria. The Examiner stated that "*Gupta* does not expressly teach using the SUIF system's program transformation and optimization features to modify a program in response to a comparison of memory usage statistical data and one or more design criteria." (May 20, 2004 Office Action, Page 14, Lines 8-10). The Examiner asserted that this deficiency of *Gupta* may be remedied by combining the *Prete* reference and the *Dutt* reference in order "to improve performance of a program." (May 20, 2004 Office Action, Page 14, Lines 19-20). The Applicant respectfully submits that the supposed motivation to combine the three references is legally insufficient for the reasons that have been previously set forth. The desire to obtain "to improve performance of a program" is too general and vague to provide the requisite motivation to modify a reference or to combine reference teachings.

For the reasons set forth above, a *prima facie* case of obviousness against Claims 2-4, 7, 9-11, 14, 16-18, 21, 23-25 and 28 has not been established. Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejections and full allowance of Claims 2-4, 7, 9-11, 14, 16-18, 21, 23-25 and 28.

V. CONCLUSION

The Applicant respectfully asserts that all pending claims in the application (Claims 1-29) are in condition for allowance and respectfully requests an early allowance of such claims.

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PATENT

SUMMARY

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: Aug 20, 2004

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